REMARKS

Claims 1-17 are pending. Claims 2 and 10-12 are being amended.

The drawing was objected to because it was not labeled "Figure 1." The applicants respectfully traverse this objection because the Rules require the drawing to not be labeled. Specifically, 37 CFR § 1.84(u)(1) states, "Where only a single view is used in an application to illustrate the claimed invention, it must not be numbered and the abbreviation "FIG." must not appear." Accordingly, the original drawing is correct as filed.

The specification was objected to because the Examiner asserted that Figure 1 should be listed in the Brief Description of the Drawings section. As discussed above, the single drawing provided with the application cannot be labeled "Figure 1" according to Rule 84(u)(1). As a result, "Figure 1" is correctly not listed in the Brief Description of the Drawings section.

Claim 12 was rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Further, claim 12 was rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Specifically, the Examiner noted that claim 12 was not claimed to be practiced on a computer.

Claim 12 is being amended to recite that the invention is practiced on a computer as suggested by the Examiner. Such an amendment highlights the practical utility of the claimed method which performs logical fuzzy union and intersection operations. Moreover, the specification describes in detail how to make and use the invention recited in amended claim 12. Accordingly, amended claim 12 is properly enabled within the meaning of Section 112, first paragraph, and is supported by a well-established utility within the meaning of Section 101.

Claims 2 and 10 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 2 and 10 are being amended to provide proper antecedent bases for the limitations noted by the Examiner. Therefore, amended claims 2 and 10 particularly point out and distinctly claim the invention.

Claims 1 and 4-17 were rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,343,553 to Miyazawa et al. ("Miyazawa").

Miyazawa does not disclose the invention recited in claims 1 and 4-17. For example, claim 1 recites a calculation circuit that includes subtracter means receiving first and

second input data, comparator means receiving a first selection signal and a sign flag output by subtracter means and outputting a second selection signal, and first data selection means receiving the first and second input data and the second selection signal and outputting a second output datum correlated to one of the first and second input data as a function of the second selection signal.

Miyazawa does not disclose the comparator means as recited in claim 1. The Examiner correctly notes that Miyazawa refers to a calculation unit with a multiplier or divider for multiplying or dividing a difference by a one of values which is in accordance with a plus or minus sign of the difference. Miyazawa does not suggest that the multiplying or dividing involves any comparison, and especially not a comparison of a sign flag and a first selection signal for selecting a logical fuzzy union operation or a logical fuzzy intersection operation. Moreover, the Miyazawa multiplier or divider receives at input a difference and a value in accordance with a plus or minus sign, and nothing in Miyazawa suggests that the difference is a first selection signal for selecting a logical fuzzy union operation or a logical fuzzy intersection operation.

Miyazawa also does not disclose the first selection means as recited in claim 1. The Examiner notes that Miyazawa shows a data selection means in Figure 31, but nothing in Figure 31 or the accompanying text suggest a data selection means that is connected as recited in claim 1 or that performs the function of the first data selection means recited in claim 1. Specifically, claim 1 recites that the first data selection means has first and second data inputs receiving the same first and second data received by the subtracter means and a selection input connected to the output of the comparison means. The selector 391 receives the same inputs XL, XR, XO, as the subtracter 392, but does not have a selection input connected to the output of any comparison means that is connected to the output of the subtracter 392. The only element connected to the output of the subtracter 392 is the multiplier 395, but the output of the multiplier 395 is not connected to a selection input of the selector 391.

Alternatively, the comparator 393 has an output connected to an input of the selector 391, but the comparator 393 does not have an input connected to the output of the subtracter 392. Instead, the comparator 393 has an input connected to output input of a

subtracter 390 which does not have first and second inputs that receive the same first and second input data as the selector 391. Instead, the subtracter 390 has one input that receives the data input xi while none of the inputs of the selector 391 receives the data input xi.

For the foregoing reasons, claim 1 is not anticipated by Miyazawa.

Claims 4-7 depend on claim 1, and thus, are not anticipated by Miyazawa for the reasons expressed above. In addition, claim 4 further recites that the comparison means comprise identity detection means that are not disclosed by Miyazawa. The Examiner points to Figure 36 of Miyazawa as showing identity selection means but nothing in Figure 36 or the accompanying text suggests that any part of Figure 36 implements an identity function in which a second selection signal assumes a first level when a sign flag and a first selection signal are identical to each other and a second level when the sign flag and the first selection signal are different from each other. Assuming that the Examiner is suggesting that the inputs CB and FT are the sign flag and first selection signal of claim 4, the circuit 403 produces a first output o1 that is zero when FT is zero and equal to oS when FT is one, regardless of the value of CB. As such, the first output o1 cannot be the second selection signal generated by an identity detection means as recited in claim 1.

The circuit 403 also produces a second output o2 that is zero when CB is zero regardless of the value of FT. When CB is one, the second output o2 is one if FT is zero, and is also one if both FT and one of oE and oG are one. As a result, the second output o2 also cannot be the second selection signal generated by an identity detection means as recited in claim 1.

For the forgoing reasons, claims 4-6 are not anticipated by Miyazawa.

Miyazawa does not disclose the invention recited in claims 8-11. Claim 8 recites a calculation circuit with a subtracter and first and second multiplexers connected to each other in very specific ways. Although the Examiner has pointed to elements of Miyazawa that are said to be the subtracter and multiplexers recited in claim 8, the elements pointed to by the Examiner are not connected as recited in claim 8. For example, claim 8 recites that the first multiplexer has first and second data inputs that receive the same first and second input data that are received by the first and second inputs of the subtracter. The Examiner points to the coefficient setters 396, 397 as the multiplexers, but neither coefficient setter has inputs connected to the same input data

that are received by the first and second inputs of either of the subtracters 390, 392. In addition, claim 8 recites that the second multiplexer has first and second inputs coupled to a first output of the subtracter and the output of the first multiplexer, respectively. Neither of the coefficient setters 396, 397 has an input coupled to the output of the other coefficient setter.

The Examiner also states that Figure 34 shows a multiplexer means for the data selector of Figure 31, but nothing in Figures 31 and 34 show multiplexers connected as recited in claim 8. Like the coefficient setters 396, 397, neither the selector 391 of Figure 31 nor the selector 401 of Figure 34 provides a second multiplexer having a first input coupled to the output of the subtracter or a second input coupled to the output of a first multiplexer. Instead, the selectors 391, 401 have inputs connected to the data inputs xL, xR, xO and outputs of the comparators 393, 394. Moreover, neither of the selectors 391, 401 have a control input coupled to the second output of a subtracter, and thus, cannot be the first multiplexer recited in claim 8.

For the foregoing reasons, claim 8 is not anticipated by Miyazawa.

Claims 9-11 depend on claim 8, and thus, are also not anticipated by Miyazawa. In addition, claims 9-11 recite additional language that, while not identical to that of claims 1, 4, and 6, further distinguish claims 9-11 from Miyazawa for reasons similar to those expressed above for claims 1, 4, and 6.

Although the language of claims 12-17 differs from that of claims 1 and 4-11, the allowability of claims 12-17 will be apparent in view of the above discussion of claims 1 and 4-11.

Claims 2-3 were rejected under 35 U.S.C. § 103 as being unpatentable over Miyazawa in view of U.S. Patent No. 5,335,314 to Tsutsumi *et al.* ("Tsutsumi").

Miyazawa and Tsutsumi do not teach or suggest the invention recited in claims 2-3. Claim 2 depends on claim 1, and thus, includes the comparator means and first selector means that are not taught by Miyazawa as discussed above with respect to claim 1. Tsutsumi likewise does not teach or suggest the comparator means and first selector means, and the Examiner does not claim that it does. For those reasons alone, claims 2-3 are nonobvious in view of Miyazawa and Tsutsumi.

In addition, claim 2 further recites second data selection means having first and second inputs connected respectively to the outputs of the first data selection means and the subtracter means. Similar to the discussion above with respect to claim 8, neither the selectors 391, 401 nor the coefficient setters 396, 397 have inputs connected to the output of a subtracter or the output of a first data selection means.

Claim 2 also recites that the second data selection means includes a selection input receiving a third selection signal for selection of either a fuzzy output mode or a non-fuzzy output mode and an output supply a third output datum as a function of the level of the third selection signal. The Examiner admits that Miyazawa does not teach such features, but asserts that Tsutsumi supplies the missing teaching in Figs 1, 4, 11, 14, and 15 and the Abstract. However, those figures of Tsutsumi clearly show both a fuzzy output and a non-fuzzy output being provided at separate outputs of the concluder section 110 without selecting either a fuzzy output or a non-fuzzy output based on a selection signal. Thus, Tsutsumi does not teach or suggest any of the features of claim 2 that are missing from Miyazawa.

For the foregoing reasons, claims 2-3 are nonobvious in view of Miyazawa and Tsutsumi.

In summary, the prior art rejections seem to be based on the alleged disclosure of particular structures recited in the claims, without regard for the connections between the structures or the recited functions of the structures. The applicants have attempted to provides examples where the prior art fails to teach or suggest those recited connections and functions. If the Examiner continues to reject the claims based on the prior art, the applicants respectfully request that the Examiner contact the applicants' attorney for a telephone interview or point to specific parts of the figures and/or specification of the prior art that provide the recited connections and functions.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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